DEPARTMENT OF ELECTRONICS ENGINEERING

ELECTRONICS ENGINEERING LAB (PG) (MODULAR-II)

Lab Manual

Course code: ECC 508

[VLSI LAB: ROOM NO. 202, NEW ACADEMIC BUILDING]

LIST OF EXPERIMENTS

Experiment 1:

Objective: Extraction of small signal parameters of MOSFET using CADENCE Virtuoso Schematic Editor.

Theory: Applying design equation to every possible device in a circuit is difficult, particularly when there is a large number of variables involved and more devices are present. So, in order to derive such analytic design equations without losing much accuracy and to develop qualitative understanding of the circuit behavior, circuit designers use a special technique called small signal modeling. This modeling also takes care of the short channel effects of MOSFET, like Channel length modulation, body effect, sub-threshold V_{ds} conduction. Figure 1(a) shows the small-signal model for an n-channel MOSFET.

In this model, the complex MOSFET structure is represented as a set of transconductances (g_m, g_{mb}, and $1/r_o$) and the parasitic junction capacitances between each terminal. The dependent current source $g_m V_{gs}$ reflects how drain current is controlled by gate source voltage. The channel length modulation effect, which corresponds to the dependence on V_{ds} voltage source, is represented as r_o resistance. The current-source $g_{mb} V_{bs}$ reflects the body effect on the MOSFET.

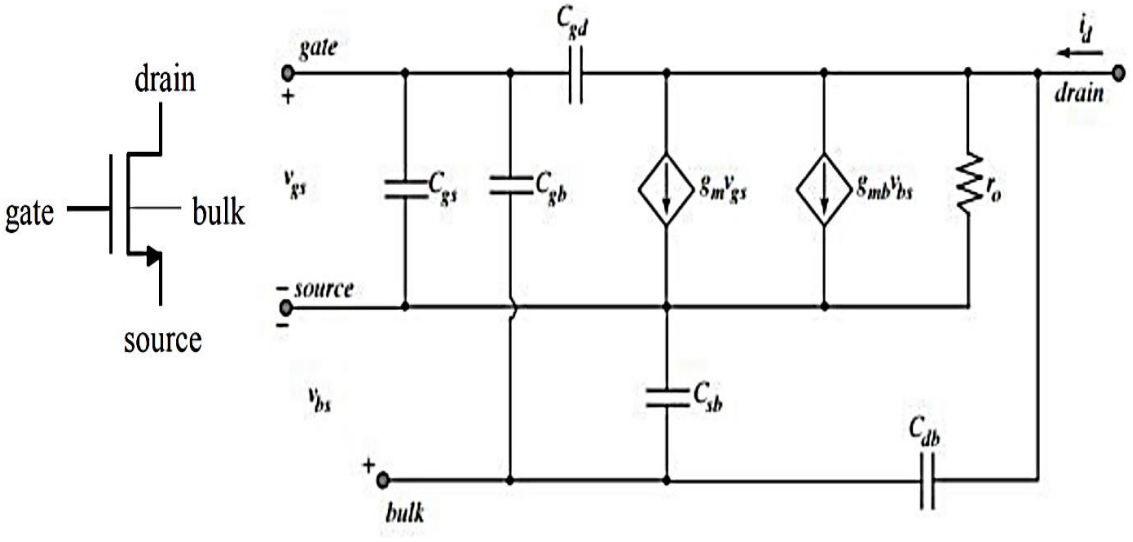


Figure 1(a): small signal model of NMOS

The parasitic junction capacitances, shown in Fig 1(a) affects the behavior of the MOSFET, mainly on high-frequency operation. Similar to this model, the p-channel MOSFET is modeled as shown in Figure 1(b).

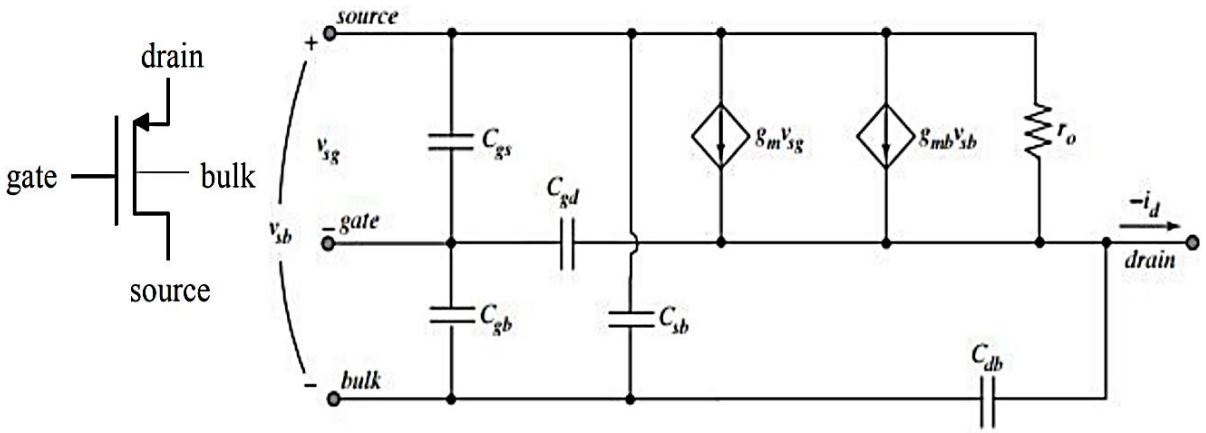


Figure 1(b): small signal model of PMOS

Analysis: DC analysis

Observation: All small signal parameters from result browser

Conclusion:

EXPERIMENT 2:

Objective: Extraction of Threshold voltage and Transition frequency of MOSFET by varying channel lengths.

Theory:

Trans-conductance varies with square root of W/L ratio and small channel length leads to threshold voltage roll off. So, the channel length will effect the f_T (transition frequency) as well threshold voltage.

$$V_{T0}\ (short\ channel) = V_{T0} - \Delta V_{T0}$$

Where V_{T0} is the zero-bias threshold voltage calculated using the conventional long channel formula and ΔV_{T0} is the threshold voltage shift (reduction) due to the short-channel effect.

$$\omega_T = \frac{g_m}{C_{gs}}$$

ω_T is transition frequency, g_m is trans-conductance and C_{gs} is gate to source capacitance.

Assignment:

1. Plot a graph between Drain current vs Gate to Source bias and find the value of threshold voltage.
2. Perform ac analysis and find the transition frequency.

Observation:

Length	f_T

Conclusion:

EXPERIMENT 3:

Objective: Design of Basic and Cascode Current Mirrors in Cadence Virtuoso Schematic Editor.

Theory:

A current mirror is a circuit block which functions to produce a copy of the current flowing into or out of an input terminal by replicating the current in an output terminal. An important feature of the current mirror is a relatively high output resistance which helps to keep the output current constant regardless of load conditions. Another feature of the current mirror is a relatively low input resistance which helps to keep the input current constant regardless of drive conditions.

Conceptually, an ideal current mirror is simply an ideal inverting current amplifier that reverses the current direction as well. Or it can consist of a current-controlled current source (CCCS). The current mirror is used to provide bias currents and active loads to circuits. It can also be used to model a more realistic current source (since ideal current sources don't exist).

BASIC CURRENT MIRROR:

The simple current mirror can be implemented using MOSFET transistors, as shown in the figure below. We know that input transistor is operating in the saturation region because V_{DS} is greater than or equal to V_{GS}. Output Transistor will also be in saturation so long as the output voltage is larger than its saturation voltage. In this simple configuration, the output current I_{OUT} is directly related to I_{DC}.

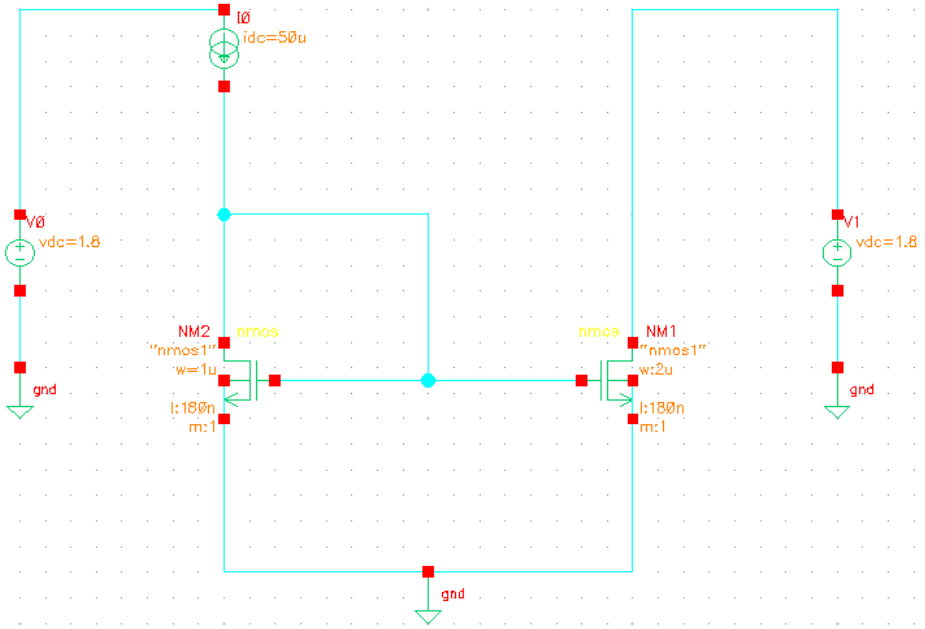


Figure 3 (a)**:** Basic current mirror circuit.

CASCODE CURRENT MIRROR:

The cascode current mirror consists of a common-source stage feeding into a common-gate stage. This topology provides a high output impedance. The matching of the load is good as the cascode configuration shields the output node.

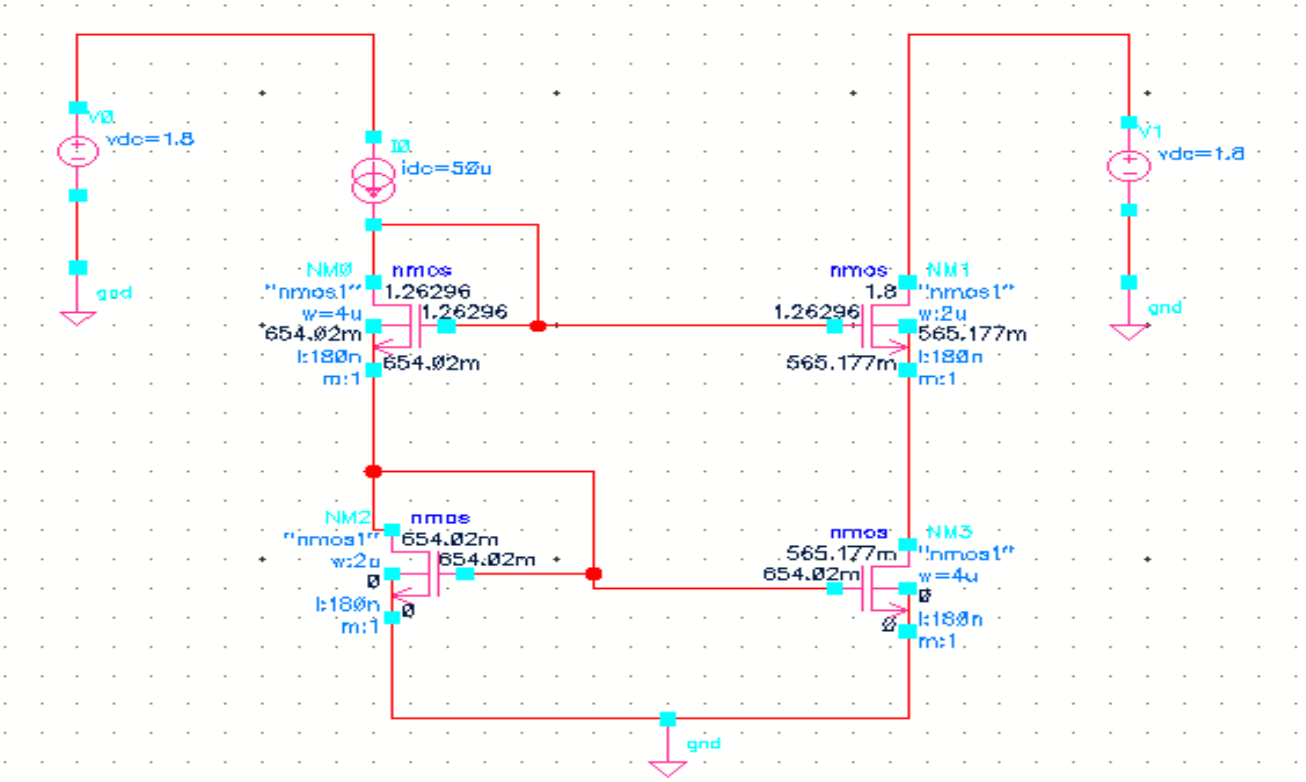


Figure 3(b): Cascode current mirror circuit

Assignment:

1. To Design a basic current mirror as shown in fig.3 (a) to provide an output current of 100 µA.
2. To Design a cascode current mirror as shown in fig. 3 (b).

Observation:

Observation table:

DC Operating points:

Parameter	Value
g_{m1}	
g_{m2}	
g_{m3}	
g_{m4}	
r_{ds1}	
r_{ds2}	
r_{ds3}	

Calculations:

Rout=

Calculated	Observed

.

Conclusion:

EXPERIMENT 4:

Objective: Design of Wilson and Regulated Cascode Current Mirrors in Cadence Virtuoso Schematic Editor.

Theory:

A current mirror is a circuit block which functions to produce a copy of the current flowing into or out of an input terminal by replicating the current in an output terminal. An important feature of the current mirror is a relatively high output resistance which helps to keep the output current constant regardless of load conditions. Another feature of the current mirror is a relatively low input resistance which helps to keep the input current constant regardless of drive conditions.

Conceptually, an ideal current mirror is simply an ideal inverting current amplifier that reverses the current direction as well. It consists of a current-controlled current source (CCCS). The current mirror is used to provide bias currents and active loads to circuits. It can also be used to model a more realistic current source (since ideal current sources don't exist).

WILSON CURRENT MIRROR

A Wilson current mirror is an improved mirror circuit configuration designed to provide a more constant current source or sink. It provides a much more accurate input to output current gain as the output resistance is higher as compared to basic current mirror. Further the negative feedback in configuration reduces the excessive current and hence maintains the output current at the desired stable value. CMOS implementation of improved Wilson current mirror is shown in Fig. 4(a).

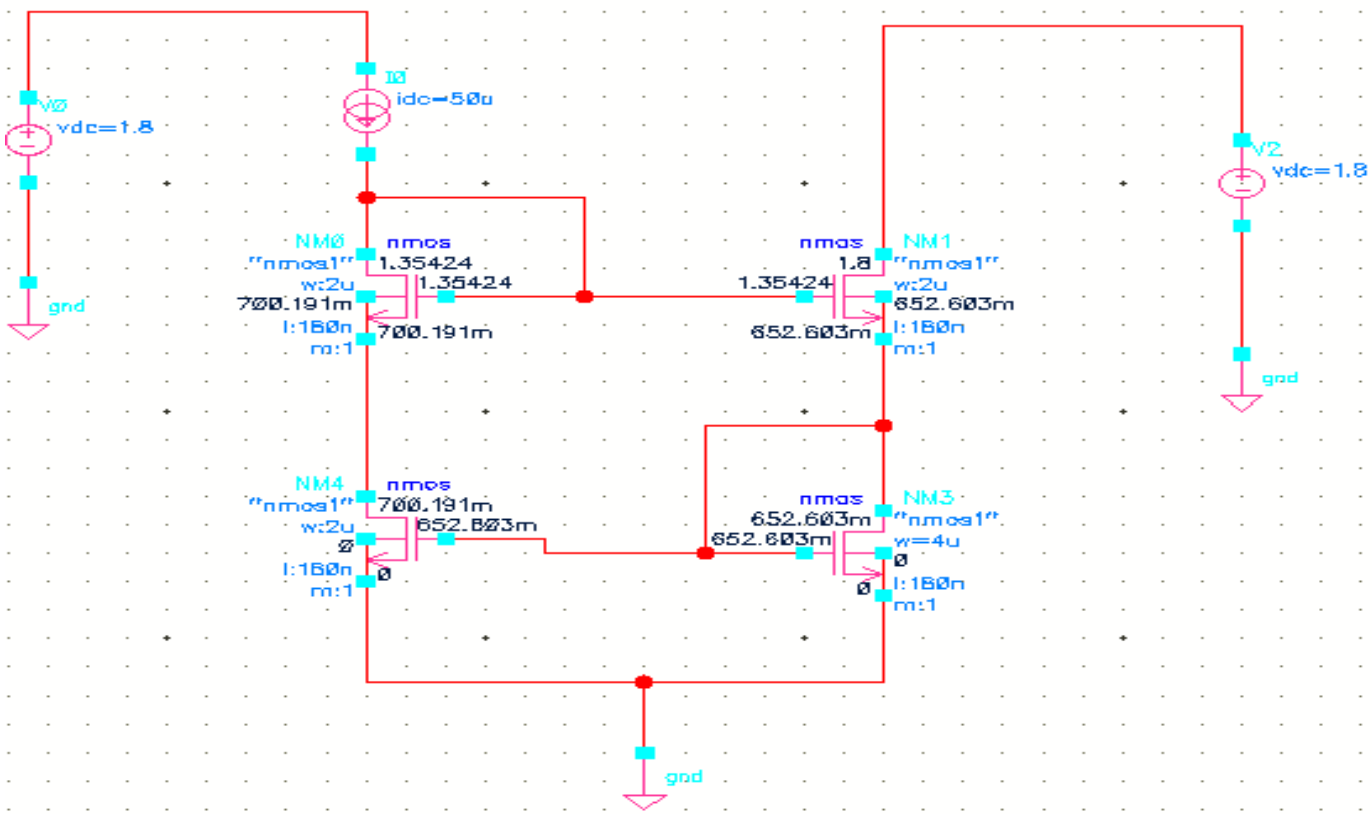


Figure.4 (a): Wilson current mirror circuit.

REGULATED CASCODE CURRENT MIRROR:

Regulated cascode current mirror is the further improvement in the cascode and Wilson current mirror circuit by providing a very high output impedance. Matching of the transistors is good as the output node is shielded thus the effect of variations at output node is reduced. A high output voltage swing is obtained in this type of topology. CMOS implementation of improved Wilson current mirror is shown in Fig. 4(b).

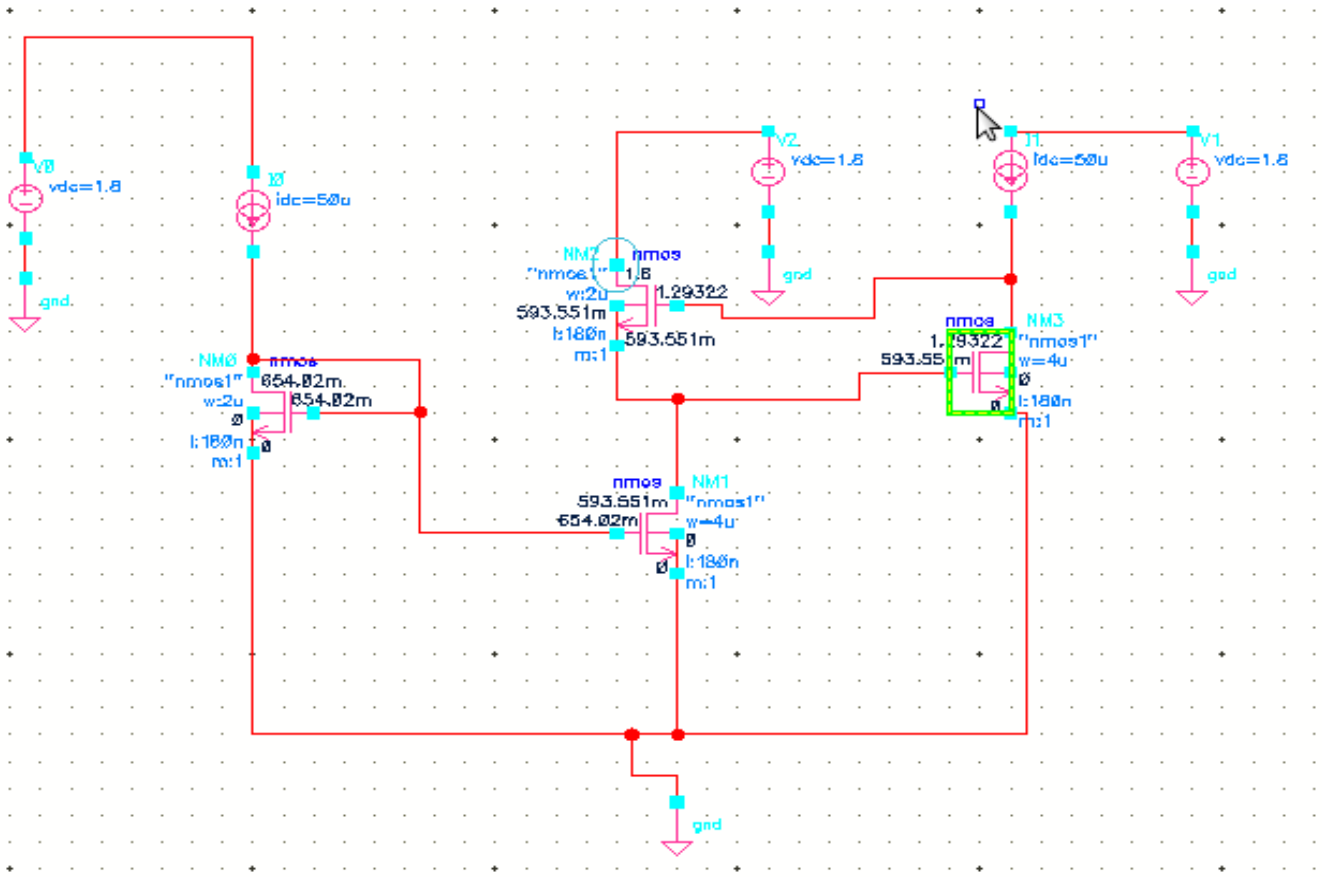


Figure 4 (b): Regulated cascode current mirror circuit.

Assignment:

1. To Design a Modified Wilson current mirror as shown in fig. 4(a) to provide an output current of 100 µA.
2. To Design a regulated cascode current mirror as shown in fig. 4(b) to provide an output current of 100 µA.

Observation:

Observation table:

DC Operating Points:

Parameter	Value
g_{m1}	
g_{m2}	
g_{m3}	
g_{m4}	
r_{ds1}	
r_{ds2}	
r_{ds3}	

Calculations:

Rout=

Calculated	Observed

.

Conclusion:

EXPERIMENT 5:

Objective: Design of Single stage amplifiers (common source with diode connected and current source load) in Cadence Virtuoso Schematic Editor.

Theory: In electronic circuits, amplifiers are used to increase the strength or amplitude of the input signal without any phase change and frequency. Amplifier circuits are made up of either FET (Field Effect Transistor) or normal bipolar junction transistor-based on their 3 terminals. The advantage of amplifier circuit using FET over BJTs is used as small-signal amplifiers because they produce high input impedance, high voltage gain, and low noise in the input signal. FET is a voltage-controlled device with three terminals -source, drain, and gate. Based on these terminals, FET is divided into 3 amplifier configuration that corresponding to 3 configurations of Bipolar transistors. They are common-source, common drain (source-follower), and common-gate amplifier circuits. The common – source amplifier circuit is most widely used than any other amplifier circuits because it can produce high input and output impedance, and also its performance is high.

When the input signal is applied at the gate terminal and source terminal, then the output voltage is amplified and obtained across the resistor at the load in the drain terminal. This is called a common source amplifier. Here source acts as a common terminal between the input and output.

The purpose of this amplifier is, it can be used as either a transconductance amplifier or a voltage amplifier. It can provide high power gain, medium current, and voltage gains according to the input and output impedances.

If the amplifier is working as a transconductance amplifier, then the input signals are amplified and modulate the current flowing to the load. If the amplifier working as a voltage amplifier, then the input signal is amplified and modulates the current passing through the FET and changes the voltage across the load resistor according to the Ohm's law.

The Schematic:

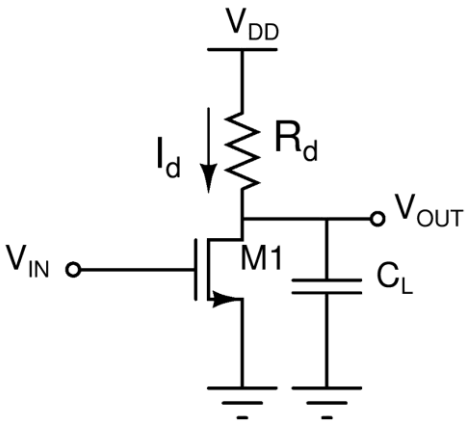


Figure 5(a): Common source amplifier with resistive load.

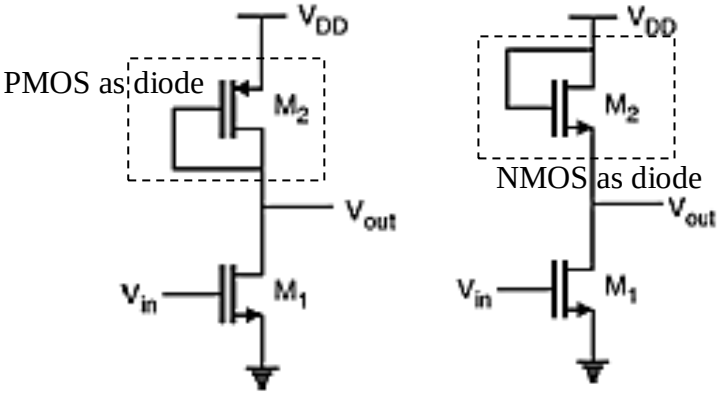


Figure 5(b): Common source amplifier with diode load

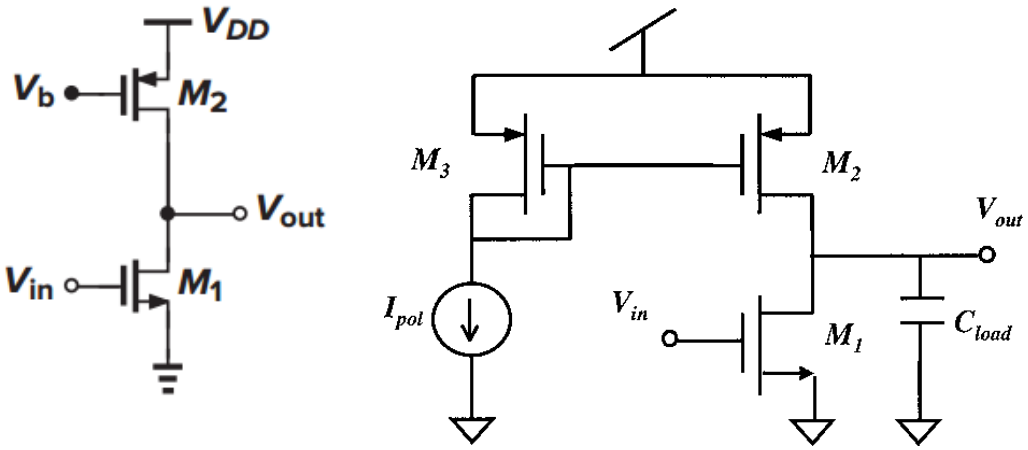


Figure 5(c): Common source amplifier with current source load

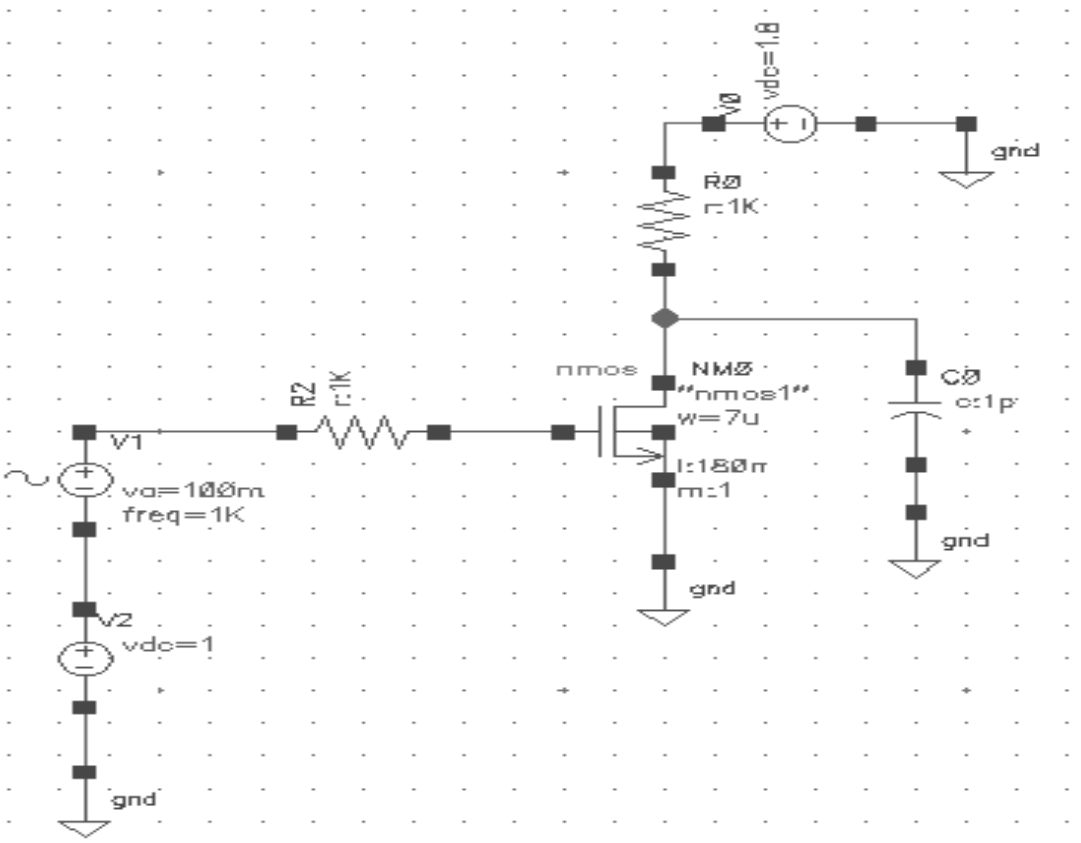


Figure 5(d): Cadence-Virtuoso schematic of common source amplifier with resistive load

Analysis: For common source with diode connected and current source load

I. Transient analysis
II. DC analysis
III. AC analysis

Observations:

I. Transient response
II. Voltage transfer characteristics
III. DC operating point
IV. Gain
V. Bandwidth
VI. Gain-Bandwidth product

Conclusion:

EXPERIMENT 6:

Objective: Design of Single stage amplifiers (cascode and source followers) in Cadence Virtuoso Schematic Editor.

Theory: Amplification is an essential function in most analog and many digital circuits.

NOTE TO DO HAND CALCULATION:

1. Use the expression of the unity-gain bandwidth (*GBW*) to calculate the small signal trans-conductance (g_m) of the input transistor.
2. Choose a usual value for the V_{DSat}voltage of the input transistor (e.g. 200 mV).
3. From the definition of the trans-conductance, a function of the drain current and the V_{DSat}voltage, determine the current flowing through the amplifier.
4. Calculate the geometry, (*W*/*L*) of the transistor by considering V_{Dsat}*and*V_{th}=0.5 V *(You can also verify the values of threshold voltage from DC operating point)*. Also determine the DC component of the input voltage $V_{in,CM}$, required for biasing.
5. Choose the DC component $V_{out,DC}$of the output voltage approximately equal to $V_{DD}/2$ in order to maximize the output voltage swing and to avoid clipping.
6. From $V_{out,DC}$and the current through the amplifier, calculate the load resistance, R_0.

Assignment:

A. By using gpdk 180 model file, design an amplifier given in Fig. 6(a) for *GBW*>20 MHz and C_L= 1 pF. In order to fulfill the design specification in spite of the parasitic effects (capacitances, g_{mb}), the parameters should be considered 1.5–2 times larger (for example, use *GBW*=30 MHz in hand calculations).

Take the supply voltage **V_{DD}=1.8 V**, channel length as **0.36 µm.**

1. Estimate the output voltage range of the amplifier and validate the found values by plotting the DC transfer characteristics, V_{out}vs. V_{in}.
2. Plot the magnitude and phase responses of the amplifier. Measure A_0 *(DC Gain)*, the frequency of the dominant pole (f_p=*BW*) and the unity gain bandwidth *GBW*.
3. Simulate the transient response of the amplifier for a sine wave input with 1 KHz frequency and the amplitude set to 5 mV, 10 mV and then 20 mV.

Measure the output amplitude for a 20 mV input voltage? Is the output voltage clipped/distorted?

Test Schematic:

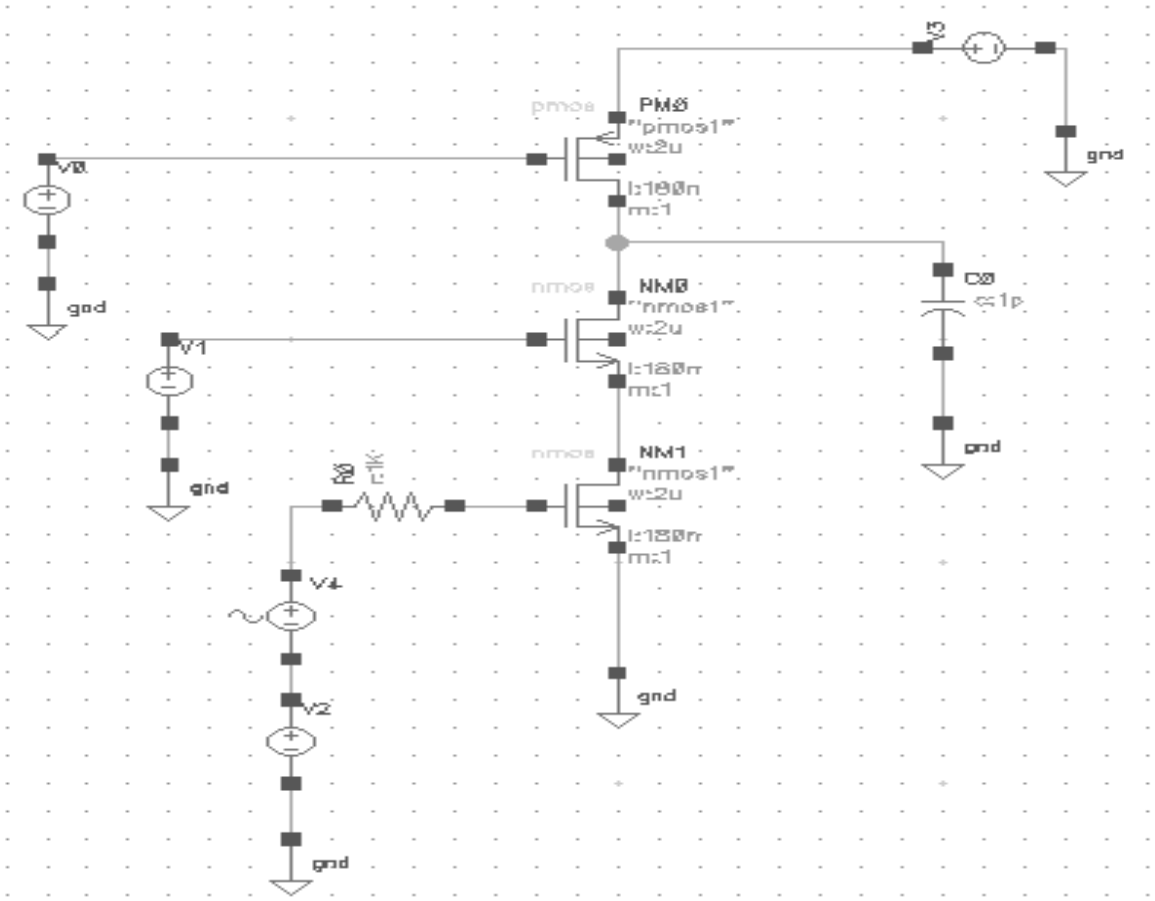
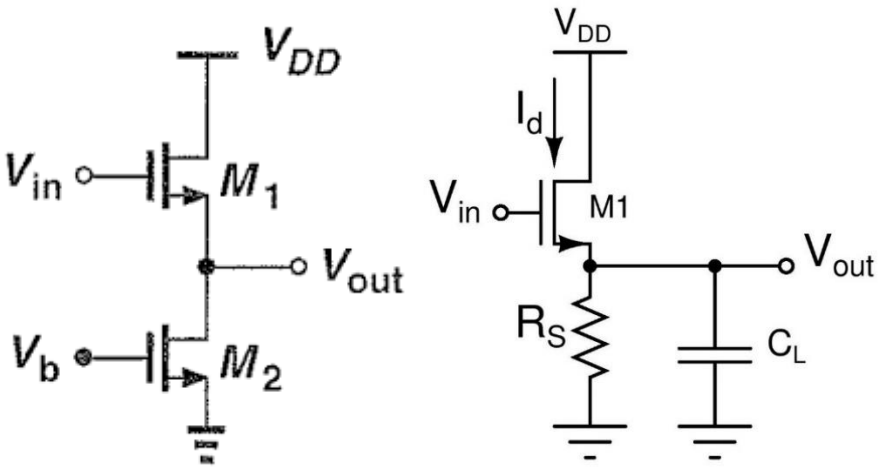


Figure 6(a): Common source amplifier with cascode input stage.

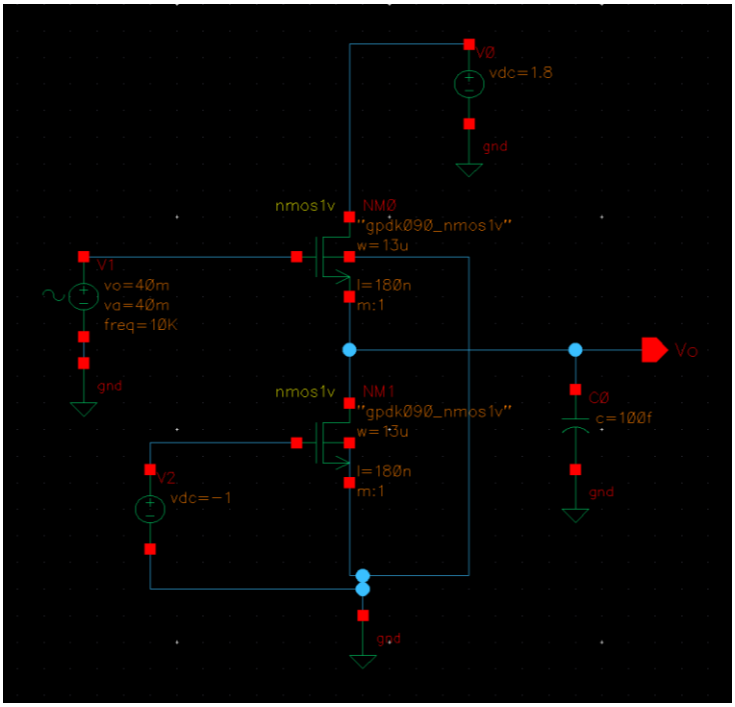
B. By using gpdk 180 model file, design an amplifier given in Fig. 6(b) for *GBW*>20 MHz and C_L= 1 pF. In order to fulfill the design specification in spite of the parasitic effects (capacitances, g_{mb}), the parameters should be considered 1.5–2 times larger (for example, use *GBW*=30 MHz in hand calculations). Either generate bias using current mirrors or apply DC bias voltages directly to NM0, PM0 and PM1 for DC biasing of the amplifier.

Take the supply voltage **V_{DD}=1.8 V**, channel length as **0.36 um.**

Follow the steps given for problem A. Repeat the steps 1 to 3 of problem A for B.



(i) (ii)



(iii)

Figure 6(b): Source follower amplifier, (i) Biased current source load (ii) Resistive load. (iii) CMOS implementation in cadence virtuoso.

Observation:

Conclusion:

EXPERIMENT 7:

OBJECTIVE: Design of Differential amplifiers (current source load and active current mirror load) in Cadence Virtuoso Schematic Editor.

THEORY:

A differential amplifier amplifies the difference between two input voltages but suppresses any voltage common to the two inputs. It is an analog circuit with two inputs V_{in}^- and V_{in}^+ one output V_{out} in which the output is ideally proportional to the difference between the two voltages.

$$V_{out} = A(V_{in}^+ - V_{in}^-)$$

where A is the gain of the amplifier.

ASSIGNMENT:

A. By using gpdk 180 model file, design an amplifier given in Fig. 1 for Gain >=20 dB, *GBW*>=20 MHz, Power dissipation<=50 µW. Consider load capacitance, C_L= 1 pF. In order to fulfill the design specification in spite of the parasitic effects (capacitances, g_{mb} etc.), the parameters should be considered 1.5–2 times larger (for example, use Gain= 26 dB, *GBW*=30 MHz and Max. Power dissipation = 50 µW in hand calculations).

Take the supply voltage **V_{DD}=1.8 V**, channel length as **0.36 µm.**

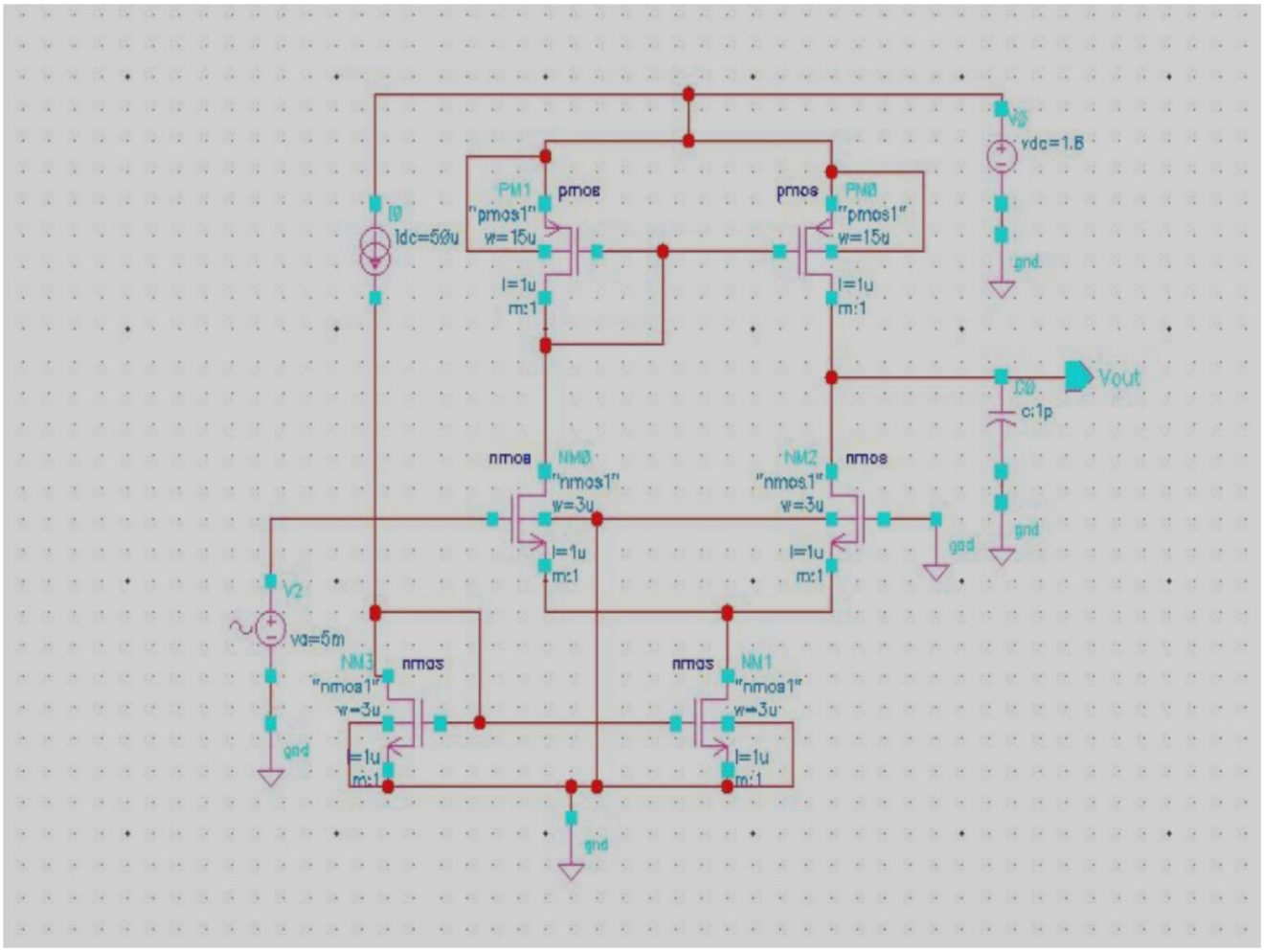


Figure 9(a): Single ended Differential amplifier with current source load.

For the above circuit, make the following analysis:

1. **Transient Analysis**
2. **DC Analysis**
   Turn on the **component parameter**, double click the **select component**
   Select input signal **Vsin** for dc analysis
3. **AC Analysis**

Execute outputs to be plotted. Click on the output net and input net.

Calculations:

i) Calculate the gain of diff. amp.
ii) Calculate the 3-dB bandwidth and GBW
iii) Calculate the CMRR.
iv) Verify with the hand calculations.

B. For the same specifications given in (A) above, repeat the same sets of analysis for the schematic in Fig. 2.

Calculations:

i) Calculate the gain of diff. amp.
ii) Calculate the 3-dB bandwidth and GBW
iii) Calculate the CMRR.
iv) Verify with the hand calculations.

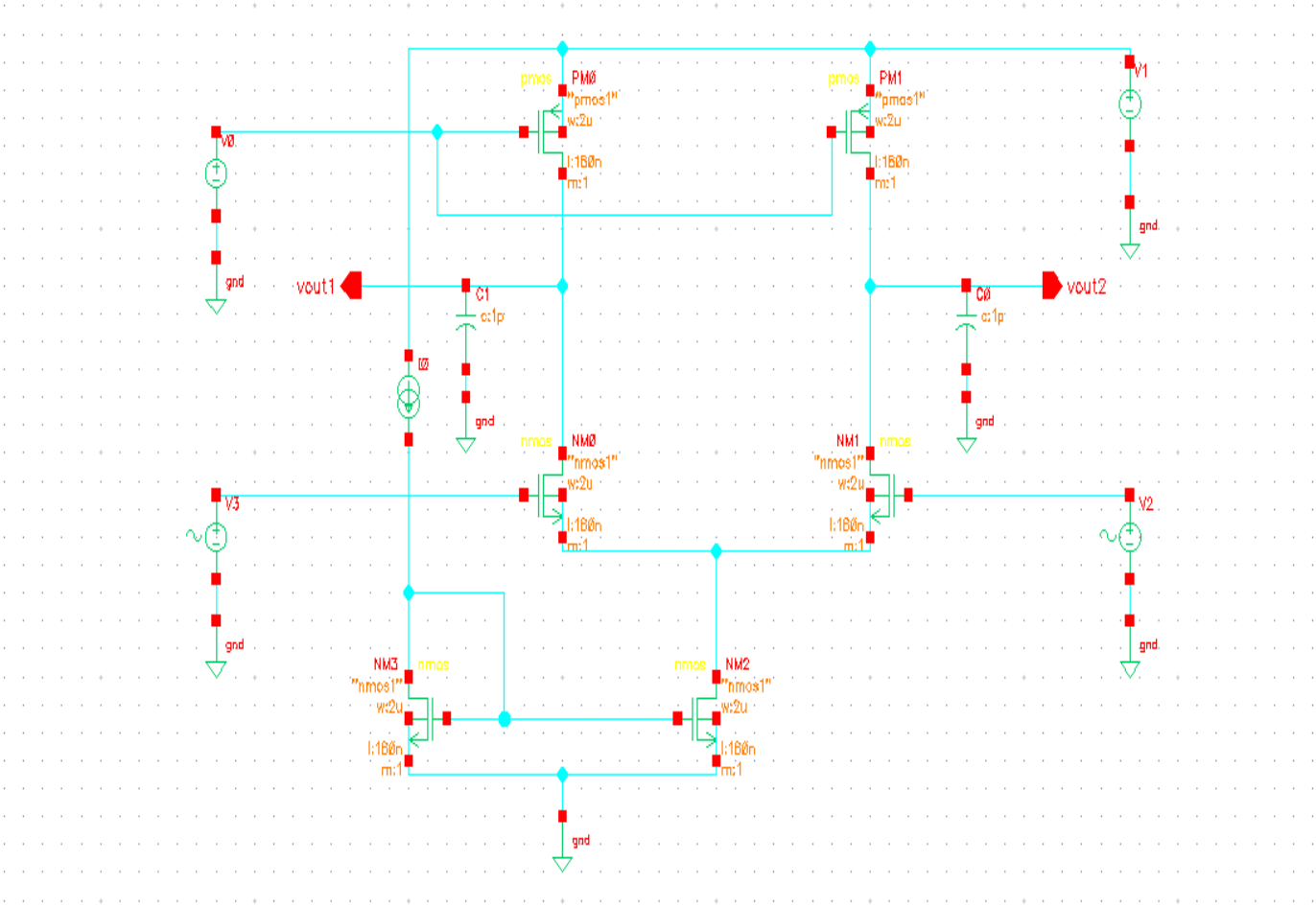


Figure 9(b): Double ended Differential amplifier with current source load.

Observation:

Conclusion:

EXPERIMENT 8:

OBJECTIVE: Design of Differential amplifiers (telescopic cascode and folded cascode) in Cadence Virtuoso Schematic Editor.

THEORY:

A differential amplifier is a circuit which is designed to amplify the difference input available and reject the common-mode voltage. It is used for suppressing the effect of noise at the output. Since the noise present will be having the same amplitude at the two terminals of the op-amp. Differential amplifier is an important building block in integrated circuits of analog system. In simple words, we can say it is a device that amplifies the difference of 2 input signals.

There are various types of differential amplifier to achieve high gain. Telescopic and folded cascade differential amplifiers are among them. The basic circuit diagrams of these amplifiers are shown in Fig. 8(a) and 8(b).

The Schematic:

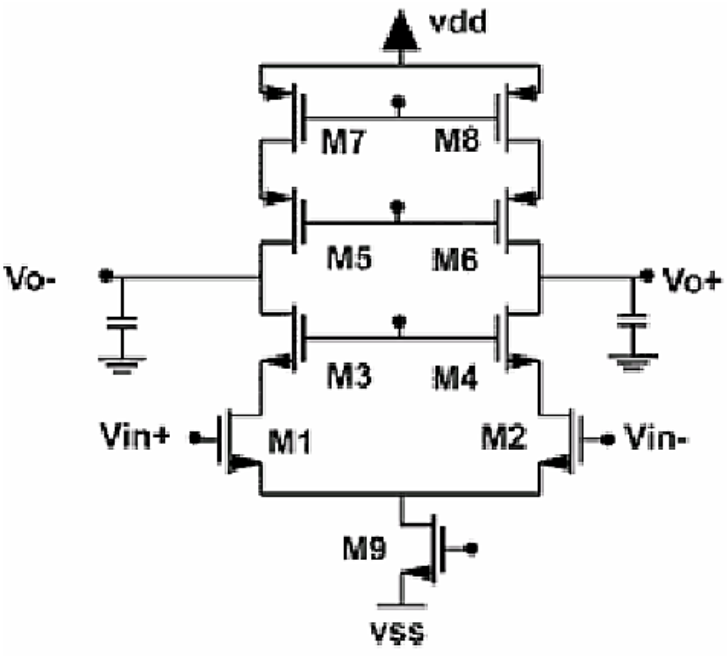


Figure 8(a): Telescopic differential amplifier

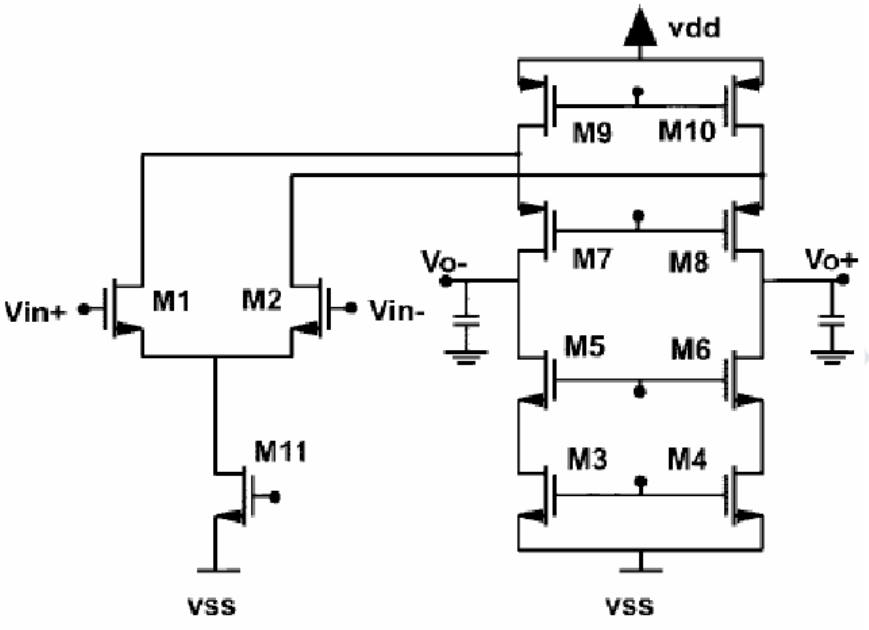


Figure 8(b): Folded cascode differential amplifier

Analysis: Forcommon source with diode connected and current source load

I. Transient analysis
II. DC analysis
III. AC analysis

Observation:

i) Gain
ii) 3-dB bandwidth
iii) GBWP (Gain-Bandwidth Product)
iv) CMRR (Common Mode Rejection Ratio)

Conclusion:

EXPERIMENT 9:

Objective: Design of Operational Amplifiers in Cadence Virtuoso Schematic Editor.

Theory: An operational amplifier is a DC-coupled high-gain electronic voltage amplifier with a differential input and, usually, a single-ended output. In this configuration, an op-amp produces an output potential (relative to circuit ground) that is typically much higher than the potential difference between its input terminals. Operational amplifiers had their origins in analog computers, where they were used to perform mathematical operations in many linear, non-linear, and frequency-dependent circuits.
An ideal op-amp is usually considered to have the following characteristics:

1. Infinite open-loop gain $G = V_{out} / V_{in}$
2. Infinite input impedance R_{in}
3. Zero input offset voltage
4. Infinite output voltage range
5. Infinite bandwidth with zero phase shift and infinite slew rate
6. Zero output impedance.
7. Infinite common-mode rejection ratio (CMRR).

Assignment:

Design a two-stage OP-AMP shown in Fig. 1 by using **gpdk 180 nm** model file. Set minimum channel length as **360 nm**. Determine W, L for all devices and the value of compensation capacitor (Cc) for the following specifications:
Open loop gain > 1000 Phase Margin > 45^o.
Static power dissipation < 180 μW Slew rate: As high as you can achieve.
(Design guidelines: For the maximum slew rate, try and utilize entire static power budget to bias the first and second stage. You have a total of 100 μA bias current budget. For example you can allocate 60 μA to M5 and 30 μA to M7. Use rest of the 10 μA for MB3, MB5 branch. Then use appropriate W and L for first and second stage to get required gain. Then use appropriate Cc and nulling transistor for pole splitting and zero cancellation).

Characterize the following parameters through simulation in Virtuoso:
1. Plot open loop differential gain versus frequency (both magnitude and phase plot) using AC simulation. What is the unity gain bandwidth and what is the phase margin through simulation? What is the frequency of the dominant pole?
2. What is the input Common mode range of your OP-AMP?
3. Plot open loop common mode gain and CMRR versus frequency

4. Characterize the step response of the OP-AMP and thereby obtain the slew-rate. Obtain the step response for the following step inputs at Vi_2:

(a) 1 μV (b)1 mV (c)1 V

5. Connect a variable capacitance load at the output of the OP-AMP. Plot the variation in phase margin as a function of the value of the load capacitance.

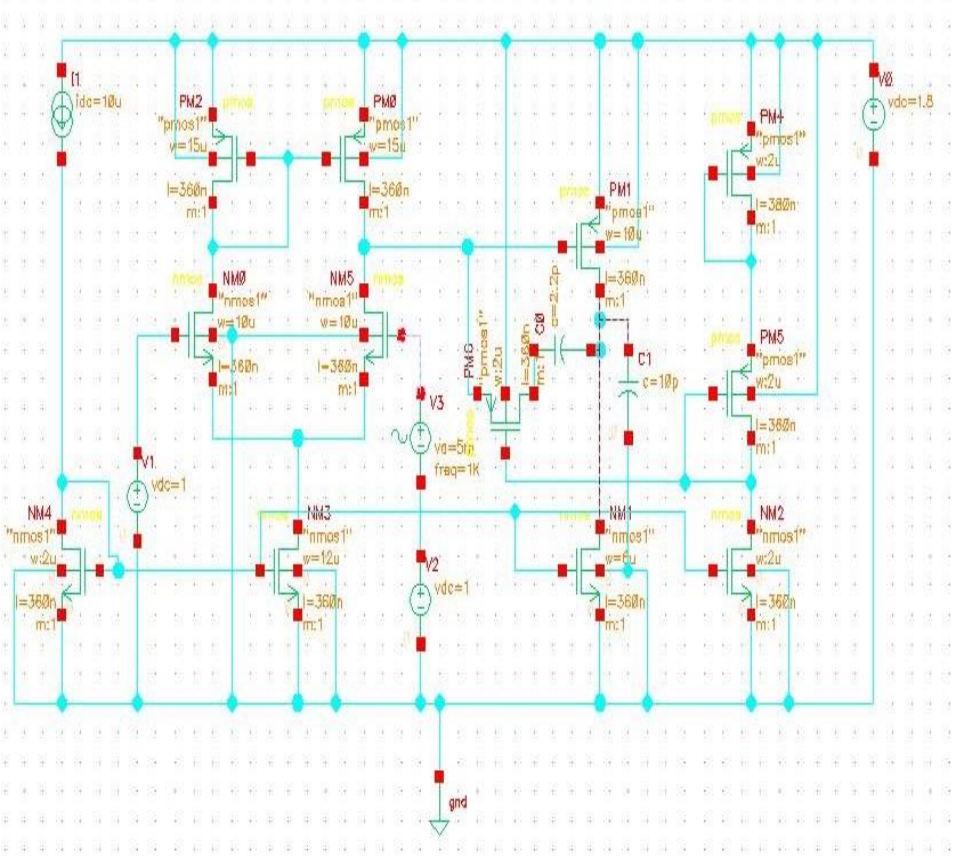


Figure 9(a): Schematic of an OPAMP

Observation:

Mention values of all the resistors and biasing of all the NMOS and PMOS used in the circuit.

Conclusion:

EXPERIMENT 10:

Objective: Design of Operational Transconductance Amplifier (OTA) in Cadence Virtuoso Schematic Editor.

Theory: The OTA is a voltage-controlled current source whose differential input voltage yields an output current by means of its transconductance (g_m). The port relationship and transconductance parameter of an OTA is given by:

$$I_O = g_m(V_{in+} - V_{in-}), g_m = \frac{k}{\sqrt{2}}(V_B - V_{SS} - 2V_{th})$$

Where k is a parameter of MOS device given by

$$k = \mu_n C_{ox} \frac{W}{L}$$

Here, μ_n denotes the carrier mobility in the channel region while W/L and C_{ox} are the aspect ratio and oxide capacitance per unit area of MOSFET, respectively.

Assignment:

Design an OTA shown in Fig. 10 by using **gpdk 180 nm** model file. Set minimum channel length as **360 nm**. Determine W, L for all devices and the value of compensation capacitor (Cc) for the following specifications:
Open loop gain = 60 dB, GB= 5MHz, C_L = 10pf.
Static power dissipation < 3 mW Slew rate: As high as you can achieve.
(Design guidelines: For the maximum slew rate, try and utilize entire static power budget to bias the first and second stage. Use an appropriate W and L to get required gain. Then use appropriate Cc and nulling transistor for pole splitting and zero cancellation).

Characterize the following parameters through simulation in Virtuoso:
1. Plot open loop differential gain versus frequency (both magnitude and phase plot) using AC simulation. What is the unity gain bandwidth and what is the phase margin through simulation? What is the frequency of the dominant pole?
2. What is the input Common mode range of your OTA?
3. Plot open loop common mode gain and CMRR versus frequency
4. Obtain gm of an OTA

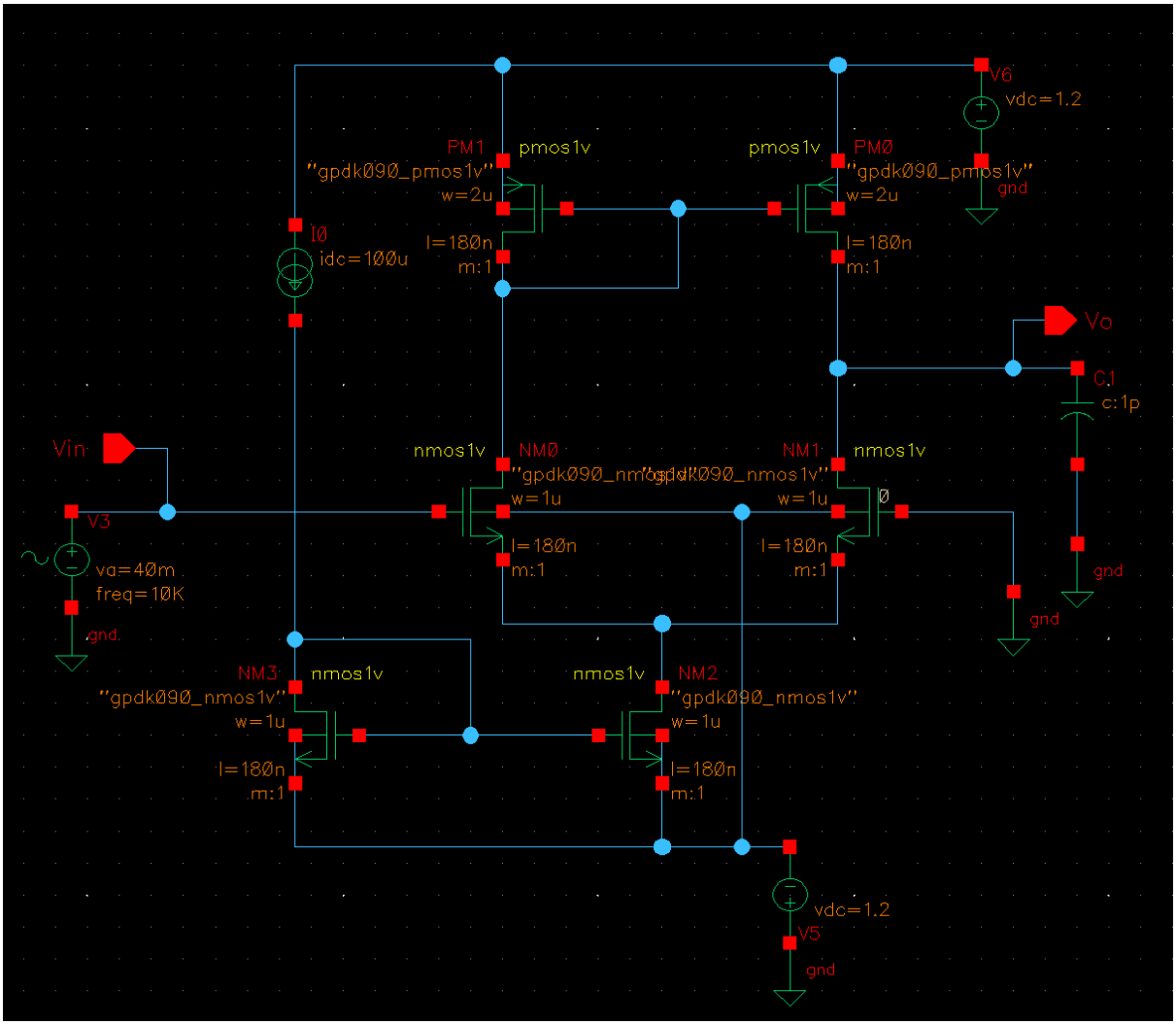


Figure 10: Schematic of an OTA

Observation:

Mention values of all the biasing of all the NMOS and PMOS used in the circuit.

Conclusion:

EXPERIMENT 11:

Objective: Noise analysis of Single stage and Differential Amplifiers designed in the previous Experiments in Cadence Virtuoso Schematic Editor.

Theory:

Noise is an unwanted disturbance in an electrical signal. Noise analysis is very important in many analog and circuits since the received signals are generally very weak.
In electrical circuits there are 5 common noise sources:
• Shot noise
• Thermal noise
• Flicker noise
• Burst noise
• Avalanche noise

Signal Stage Amplifiers:

Noise analysis is very important in many analog and circuits since the received signals are generally very weak. In single stage amplifiers the contribution of various circuit elements to noise must be taken into consideration. Resistors, MOSFETs and Diodes are the common sources of noise in analog circuits. In order to perform noise analysis we need to have accurate noise models for various elements used in the design. Since noise voltages and currents are small in magnitude, their influence on the circuit can be obtained through small signal analysis of the circuit. As a result, the noise voltages and currents can be added to the small signal model of the circuit.
The most important noise is the Thermal Noise. Rms noise due to sum of two uncorrelated noise sources e_1 and e_2 will be:

$$e_{rms} = \sqrt{\frac{1}{T}\int_0^T (e_1 + e_2)^2\, dt} = \sqrt{\frac{1}{T}\int_0^T e_1^2\, dt + \frac{1}{T}\int_0^T e_2^2\, dt + \frac{1}{T}\int_0^T e_1 e_2\, dt}$$

$$e_{rms} = \sqrt{\frac{1}{T}\int_0^T e_1^2\, dt + \frac{1}{T}\int_0^T e_2^2\, dt} = \sqrt{e_{1rms}^2 + e_{2rms}^2}$$

Thermal noise results from random motion of charge carriers within a conductor or a semiconductor due to the presence of scattering centers.

Follow these steps for analyzing noise in single stage amplifier circuit:

Step 1: Build the schematic of the single stage amplifier as shown in the figure below.

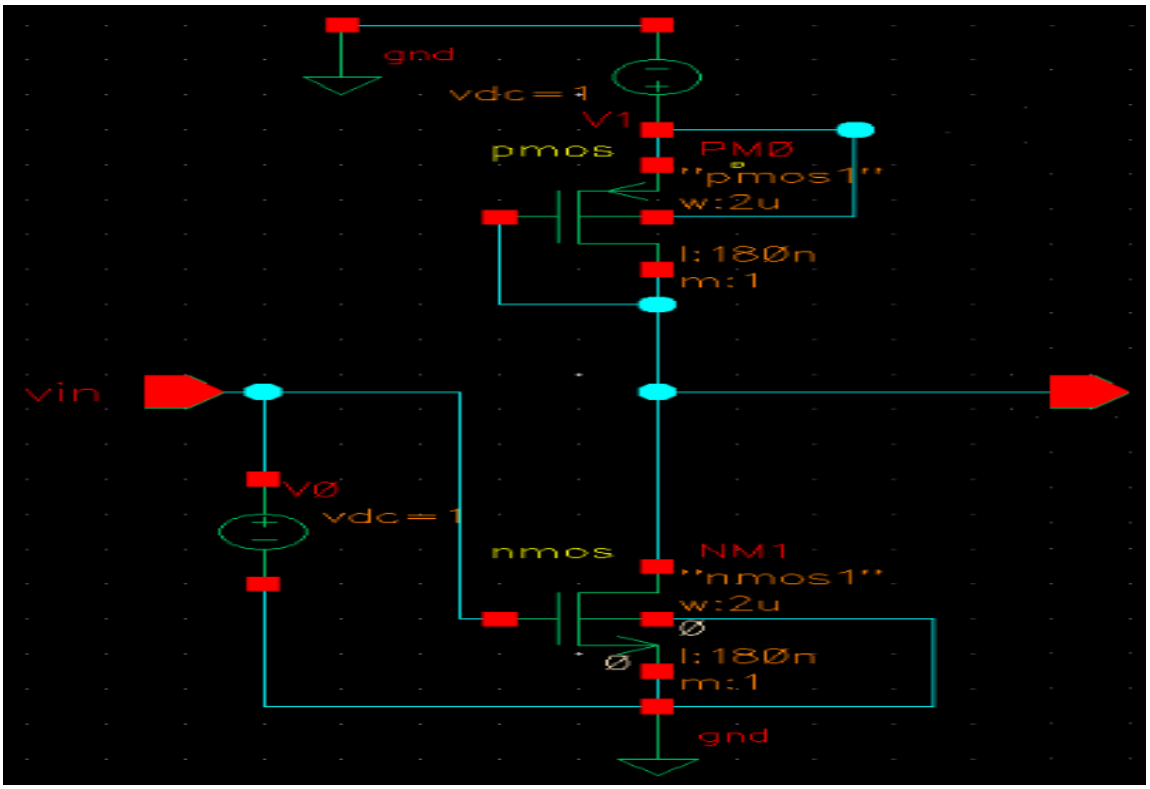
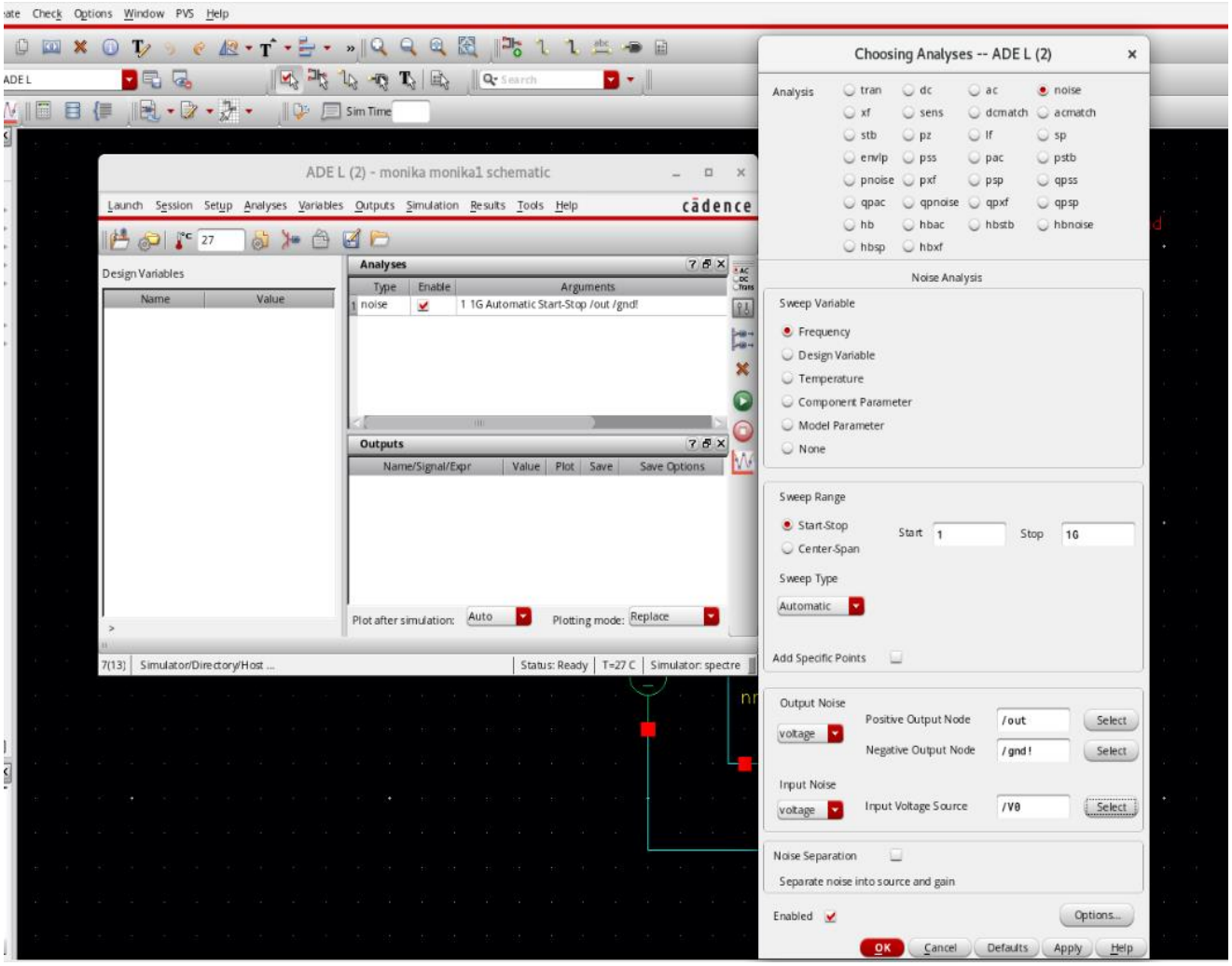


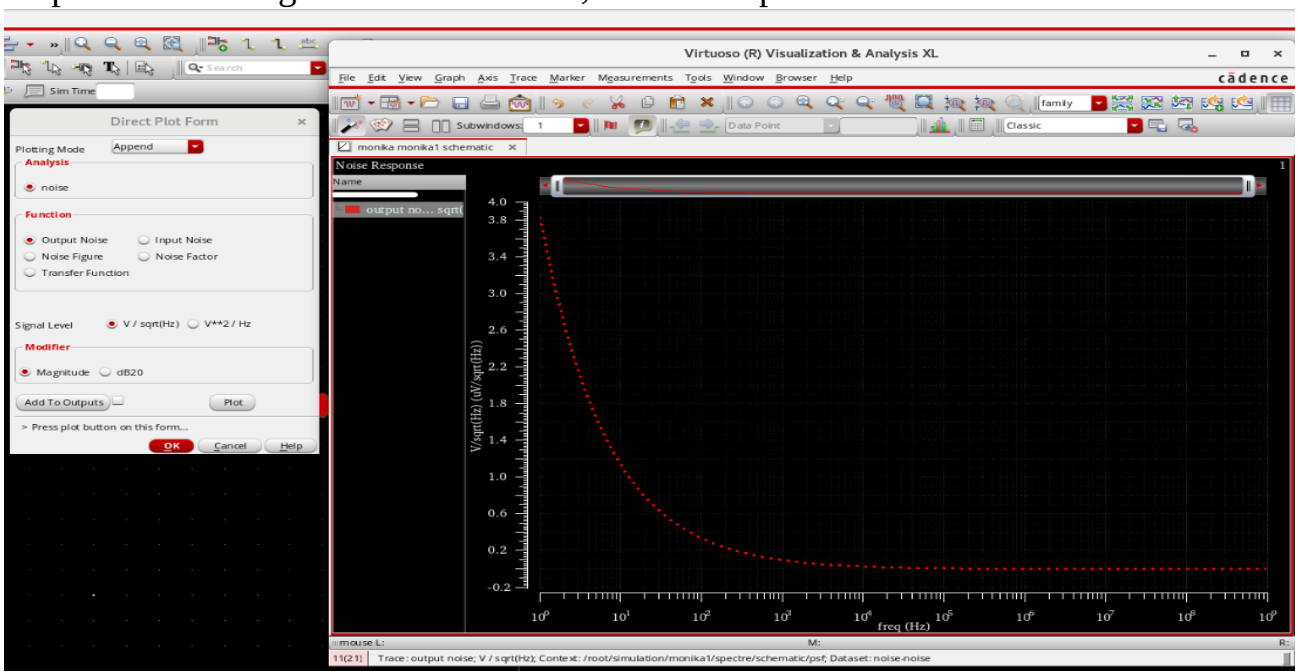
Figure 11(a): Single stage common source amplifier.

Step 2: launch ADE L and select radio button of noise from Analysis window, and fill the details as figure given below.

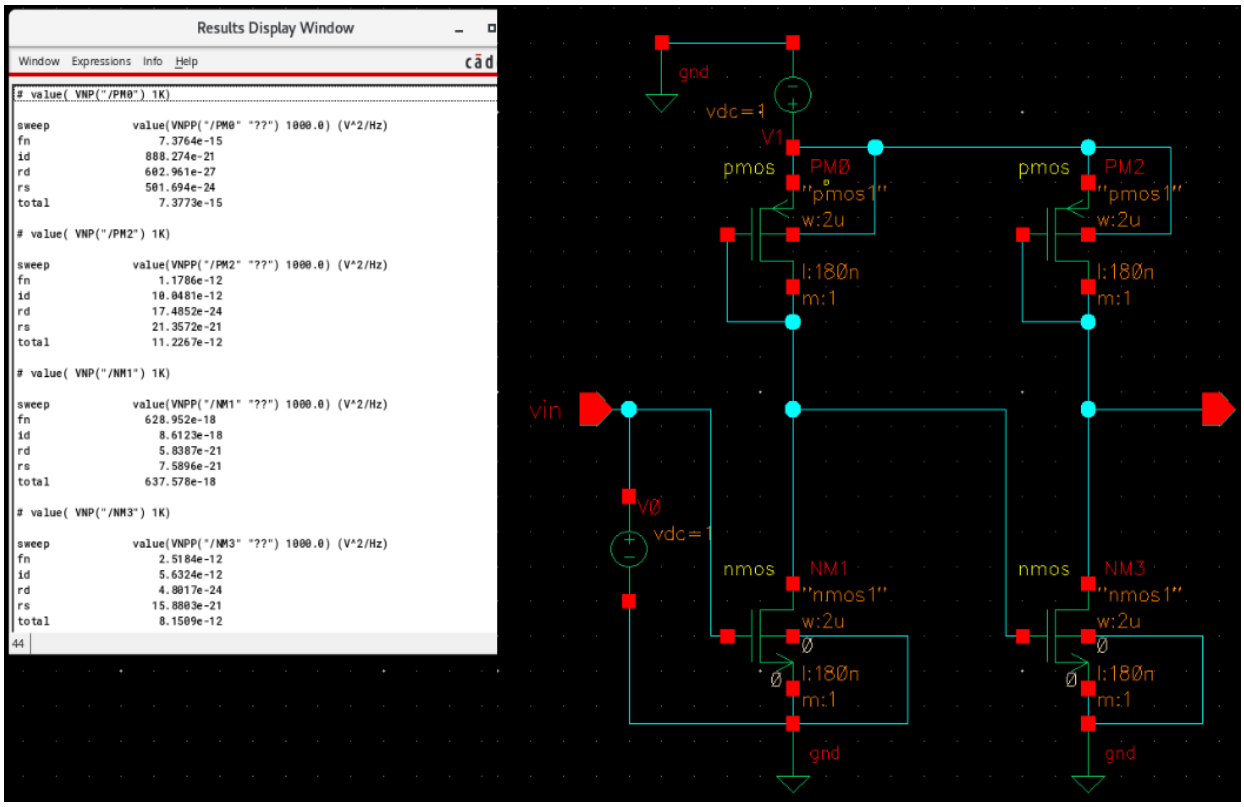
Note: Select voltage in input noise for obtaining squared voltage noise and for obtaining squared current noise, use Idc in place of Vdc and select current in input noise.



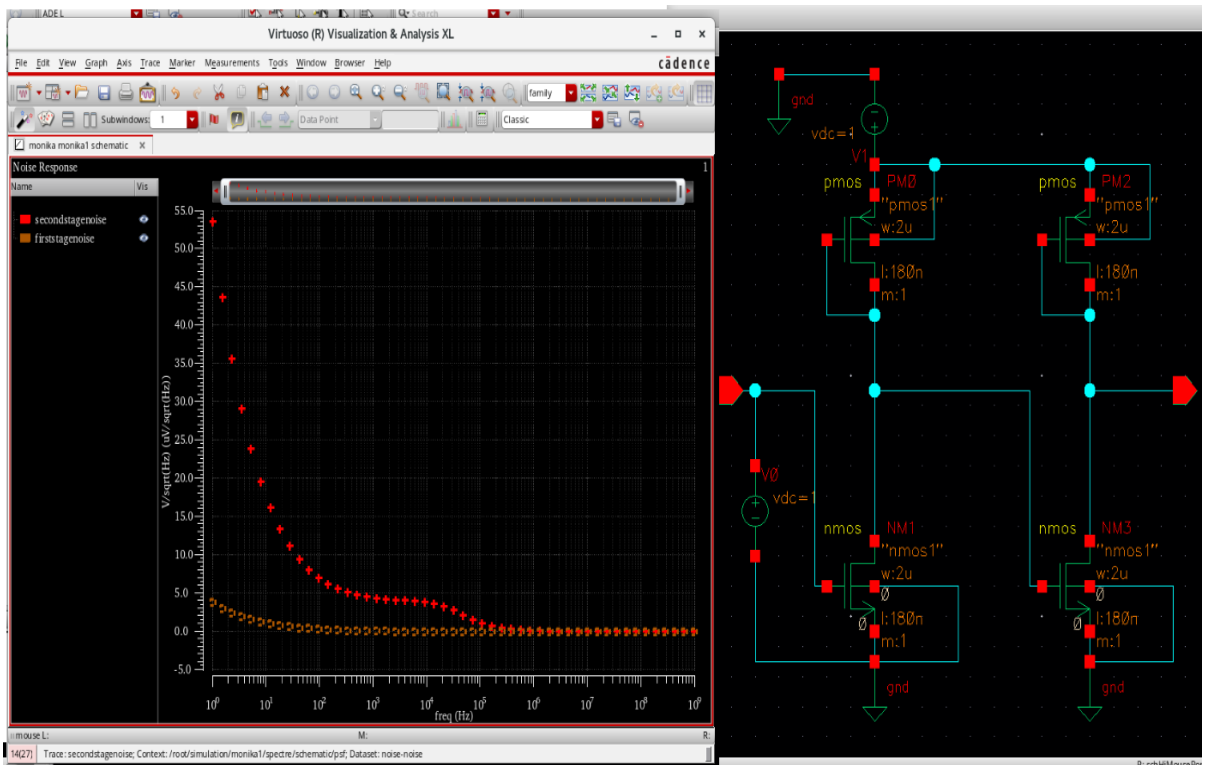
Step 3: After filling details run ADE L, see the output as follows.



Step 4: To check the contribution of noise from each MOSFET, go to results -> print -> noise summary. A dialog box will open as shown below.



Step 5: Output for first and second stage is shown below.



Assignment:

1. Obtain squared voltage noise and squared current noise of single stage amplifier and differential.
2. Find out which transistor is the maximum contributor of noise in the corresponding circuits

Observation:

Compare the noise analysis with previous results.

Conclusion:

EXPERIMENT 12:

Objective: Noise analysis of Operational Amplifier (Op-Amp) and operational transconductance amplifier (OTA) designed in the previous Experiments in Cadence Virtuoso Schematic Editor.

Theory:

Noise is an unwanted disturbance in an electrical signal. Noise analysis is very important in many analog and circuits since the received signals are generally very weak.
In electrical circuits there are 5 common noise sources:

- Shot noise
- Thermal noise
- Flicker noise
- Burst noise
- Avalanche noise

Noise in operational amplifier (Op-Amp) and OTA:

Noise analysis is an important aspect to analyze in many analog and mixed signal circuits since the received signals are generally weak due to imparted noise. In analog circuits, the contribution of various circuit elements to noise must be taken into consideration. Resistors, MOSFETs and Diodes are the common sources of noise in analog circuits. In order to perform noise analysis we need to have accurate noise models for various elements used in the design. Since noise voltages and currents are small in magnitude, their influence on the circuit can be obtained through small signal analysis of the circuit. As a result, the noise voltages and currents can be added to the small signal model of the circuit.
The most important noise is the Thermal Noise. Rms noise due to sum of two uncorrelated noise sources e_1 and e_2 will be:

$$e_{rms} = \sqrt{\frac{1}{T}\int_0^T (e_1 + e_2)^2\, dt} = \sqrt{\frac{1}{T}\int_0^T e_1^2\, dt + \frac{1}{T}\int_0^T e_2^2\, dt + \frac{1}{T}\int_0^T e_1 e_2\, dt}$$

$$e_{rms} = \sqrt{\frac{1}{T}\int_0^T e_1^2\, dt + \frac{1}{T}\int_0^T e_2^2\, dt} = \sqrt{e_{1rms}^2 + e_{2rms}^2}$$

Thermal noise results from random motion of charge carriers within a conductor or a semiconductor due to the presence of scattering centers.

Following are the steps to perform noise analysis in the circuits:

(a) Noise analysis in Op-Amp:

Step 1: Design the schematic of the operational amplifier as shown in the Fig. 12(a) below.

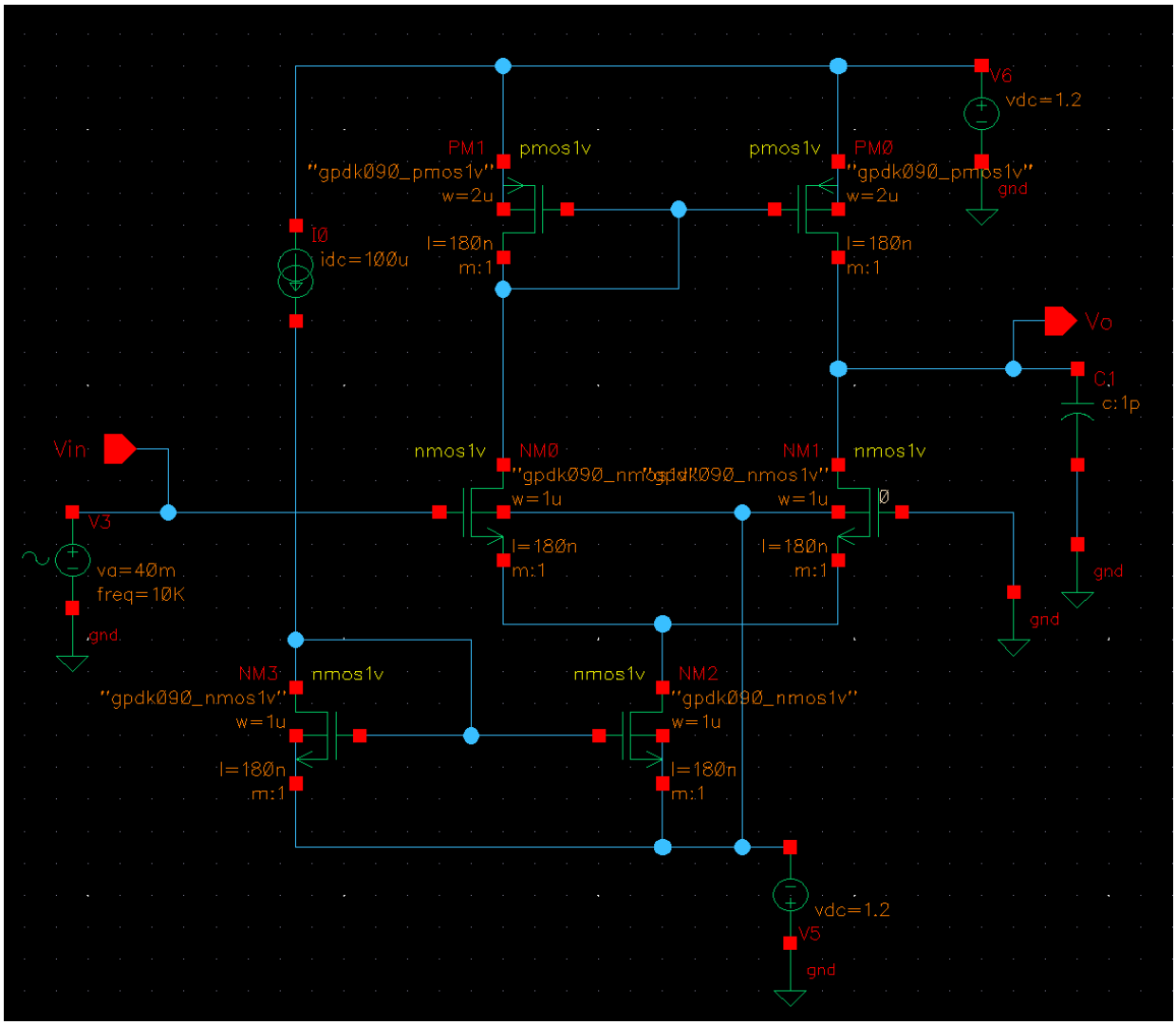


Figure 12(a): Operational Amplifier (Op-Amp).

Step 2: Launch ADE L and select noise in Analysis window, a detailed form of window will appear as Fig. 12 (b);

Figure 12(b).

Note: Select voltage in section of 'input noise' for obtaining squared voltage noise and for obtaining squared current noise, select current.

From the schematic of Fig. 12(a), select the nodes in window 12(b) as;

Positive output node: V_O

Negative output node: gnd !

Input voltage source: Vin.

Sweep the frequency from 1Hz to 1GHz.

Step 3: After filling details run ADE L, graph will result as;

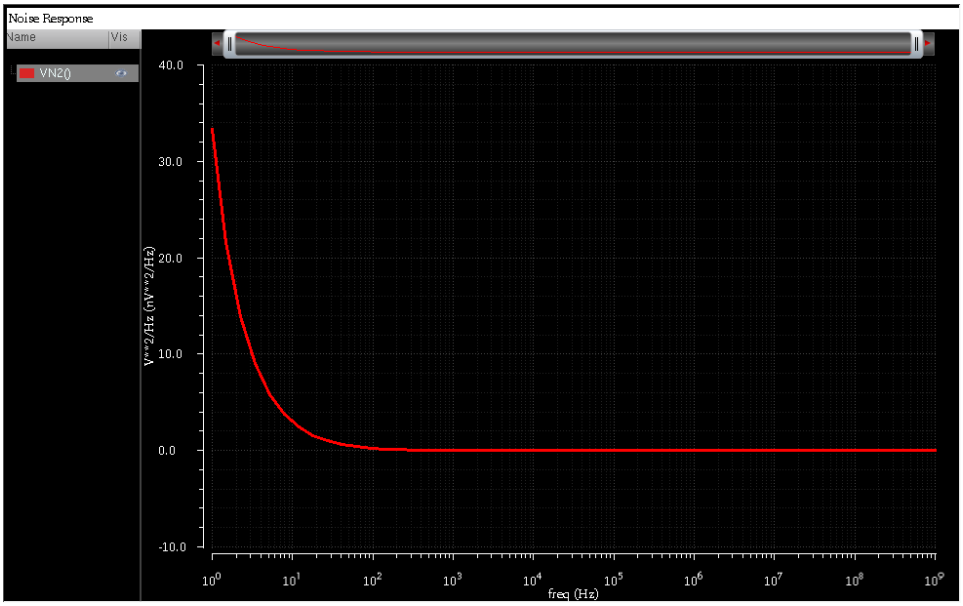


Figure 12(c).

Step 4: After running ADEL, select direct plot in the window and click on 'main form'. A main form window will appear as shown below in Fig. 12(d):

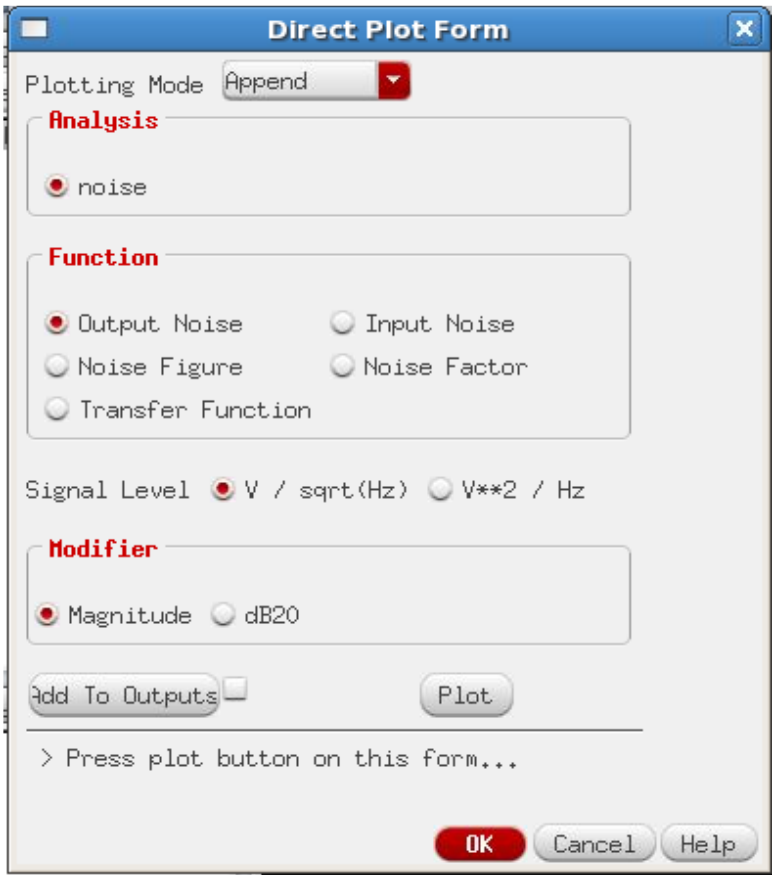


Figure 12(d).

Step 5: Click on 'plot', output referred noise (V/sqrt(Hz)) is resulted as 12(e);

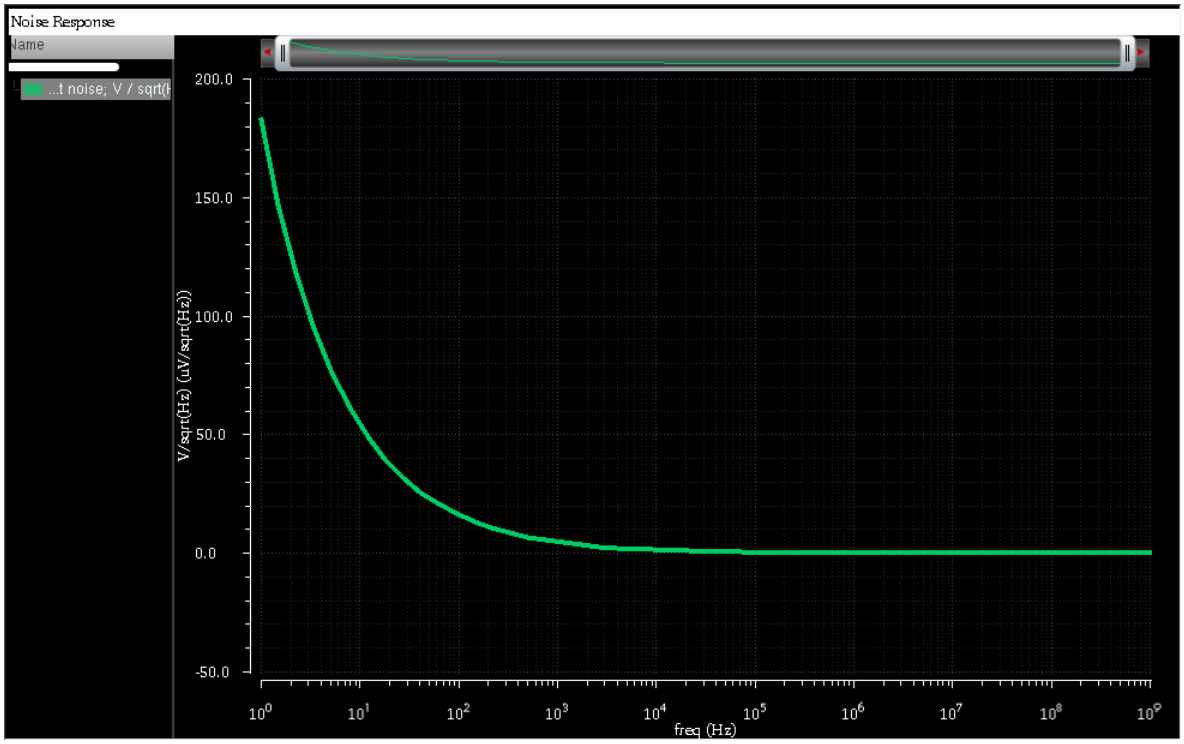


Figure 12(e).

Step 6: To check the contribution of noise from each MOSFET, go to results -> print -> noise summary. A dialog box will open as shown below and result summary will be printed.

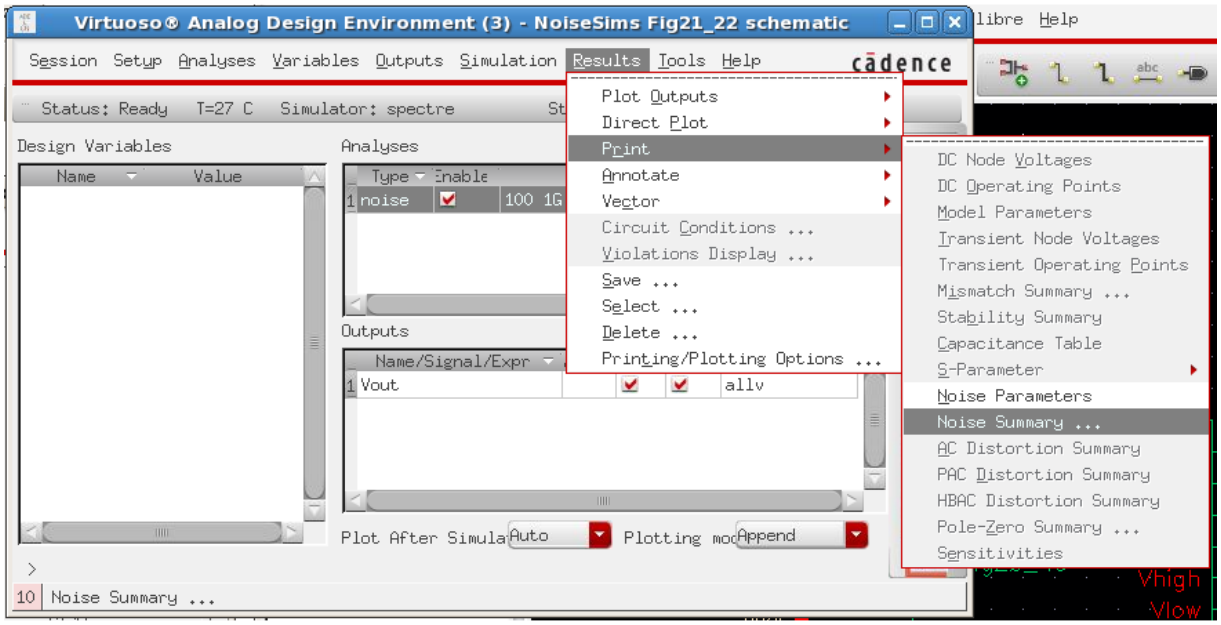


Figure 12(f).

(b) Noise Analysis of OTA:

(1) Design the CMOS structure of OTA as shown in Fig. 12 (g).

(2) Similar procedure involving all steps from 1 to 6 of analysis for Op-Amp mentioned in above section is followed to perform noise analysis in OTA circuit.

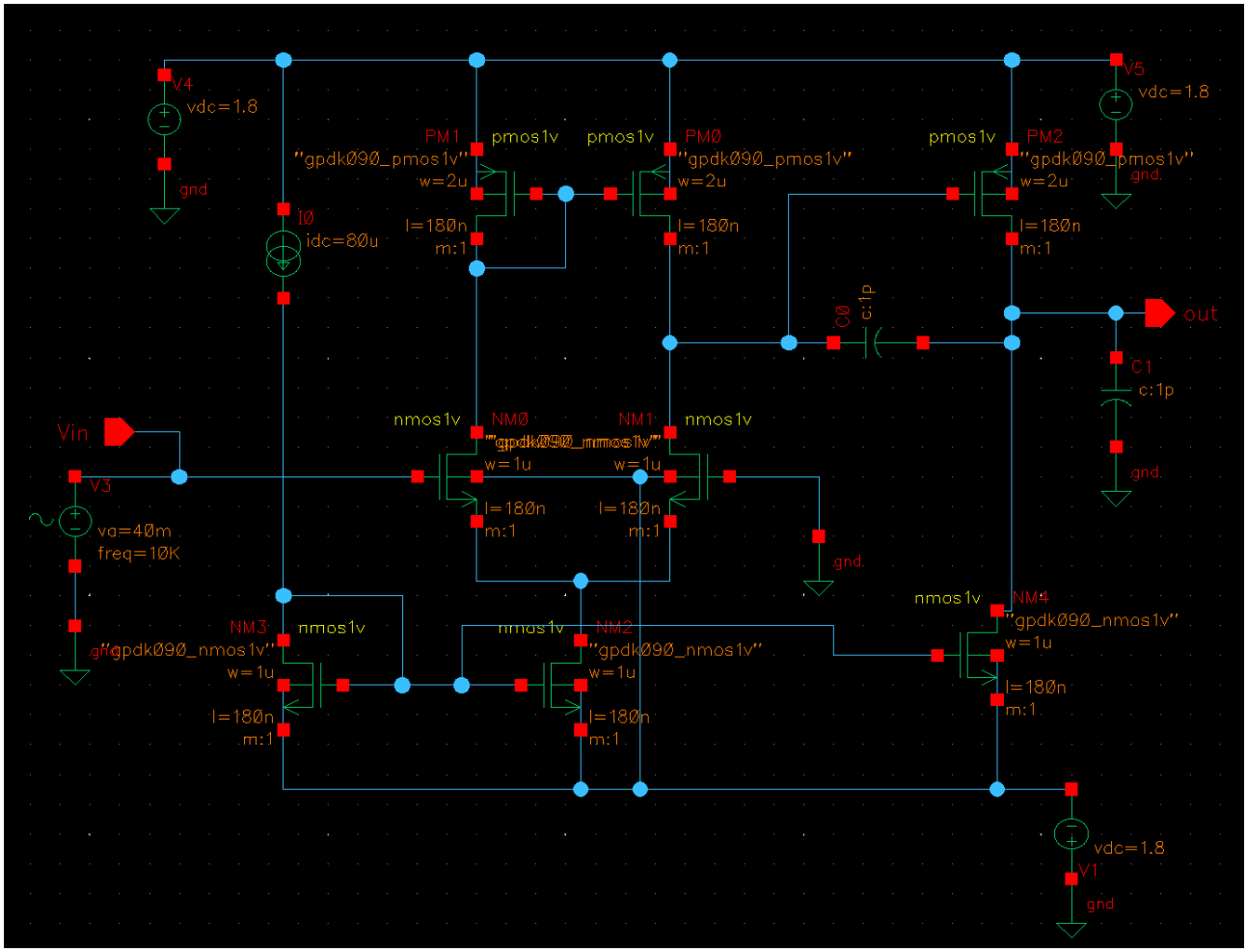


Figure 12(g): Operational Transconductance Amplifier (OTA).

Assignment:

1. Obtain squared voltage noise and squared current noise for Op-Amp and OTA following the procedure mentioned above.
2. Find out which transistor is the maximum contributor of noise in the corresponding circuits.

Observation:

Compare the noise analysis results for configurations in Fig. 12 (a) and (g).

Conclusion:

Practice Questions:

1. Why the influence of noise in OTA is less as compared to Op-Amp?
2. How does noise affect single stage circuits over double stage or multistage?
3. How does current mode circuit result advantageous over voltage mode?